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DESIGN OF A QUINARY TO RESIDUE NUMBER SYSTEM CONVERTER USING MULTI-LEVELS OF CONVERSION

Hassan Amin Osseily
Electrical and Electronics Department, Lebanese International University - Beirut Lebanon
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ABSTRACT
The objective of this paper is to present the design of a Quinary to Residue Number System (RNS) converter over the Quinary moduli set {23, 24, 25} by using Multi levels of MVL to RNS converters. This method will lead to minimize the number of used logic elements (gates, adders,..) hence reducing the propagation delay, decreasing the chip density and complexity comparing to other methods those are used in binary to RNS conversion.

KEYWORDS: Multiple Valued Logic (MVL), Residue Number System (RNS), Quinary Logic (Q_{uin}), Quinary Full Adder, QFA, Quinary Half Adder, QHA.

INTRODUCTION
The residue number system (RNS) is a non-weighted number system which speeds up the arithmetic operations by dividing them into smaller parallel operations. Since the arithmetic operations in each moduli are independent of the others, so there is no carry propagation among them and so RNS leads to carry-free addition, multiplication and borrow-free subtraction [1]. The RNS is mostly used in digital signal processing DSP and in encryption / decryption techniques for its advantages in the computation process.

One of the major issues in efficient design of RNS systems is the residue to weighted conversion and the weighted to RNS conversion. The algorithms of residue to weighted conversion are mainly based on chinese remainder theorem (CRT), mixed-radix conversion (MRC) [2] and new chinese remainder theorems (New CRTs) [2]. In addition to these methods, there are novel conversion algorithms which are designed for some special moduli sets have been proposed and discussed by other authors [3].

Multiple-valued logic (MVL) has been proposed as a means for reducing the power, improving the speed, and increasing the packing density of VLSI circuits [4]. In MVL, the number of discrete signal values or logic states extends beyond two. Arithmetic units implemented with MVL achieve more efficient use of silicon resource and circuit interconnections [5]. There is a clear mathematical attraction of using multiple-valued number representation in RNS. The modular arithmetic that is inherent in MVL can be matched with modular arithmetic needed in RNS.
The first MVL-RNS system was introduced by Soderstrand et al. [5] to design a high speed FIR digital filter. The residue to weighted converter proposed in [5] is based on chinese remainder theorem (CRT) and implemented with read-only memories (ROM's). this converter is practical to implement small and medium RNS dynamic ranges and it is not appropriate for large dynamic ranges. In [6], new RNS systems based on the moduli of forms r^a, r^b-1 and r^c+1 are presented. Abdallah et al. in [6] developed a systematic framework utilizing high-radix arithmetic for efficient MVL-RNS implementations and proposed many radix-r moduli sets. This moduli sets do not include pair-wise relatively prime moduli, and this resulting in reduced dynamic ranges and unbalanced moduli. The residue to weighted converter presented in [7] is based on CRT and because of the scale-down factors which are used for making moduli pair wise relatively prime, conversion delay and cost are increased.

BACKGROUND
A residue number system is defined in terms of a relatively-prime moduli set $\{P_1, P_2, \ldots, P_n\}$ that is GCD $(P_i, P_j) = 1$ for $i \neq j$ and $i, j = 1,2,...,n$. A weighted number X can be represented as $X = (x_1,x_2, \ldots ,x_n)$, where

$$x_i = X \bmod P_i = |X|_{P_i},\ 0 \leq x_i < P_i$$

Such a representation is unique for any integer X in the range [0, M-1], where $M=P_1P_2\ldots P_n$ is the dynamic range of the moduli set $\{P_1,P_2, \ldots,P_n\}$ [7].

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Addition, subtraction and multiplication on residues can be performed in parallel without any carry propagation among the residue digits. Hence, by converting the arithmetic of large numbers to a set of the parallel arithmetic of smaller numbers, the RNS representation yields significant speed up.

Example 1: Given the same moduli set {3, 5, 7} and the two weighted number X=32 and Y=24, their residues over the moduli set {3, 5, 7} are (2,2,4) and (0,4,3) respectively. To perform the addition and subtraction and multiplication of X and Y, we can use their residues representations as follows.
X+Y=32+24=56

The residue representation of 56 is (2,1,0)

The addition on residues
(x1,x2,x3)+(y1,y2,y3)= (2,2,4)+(0,4,3)=(2,6,7)
The residue set (2,6,7) over the moduli set (3,5,7) is equal to (2,1,0). Then we conclude that addition results are the same in the two cases of weighted and residue representation.
The algorithms of residue to weighted conversion are based mainly on Chinese remainder theorem (CRT) and mixed-radix conversion (MRC).

***Chinese Remainder Theorem*:** by CRT, the number X is calculated from residues by
$X = \left| \sum_{i=1}^{n} \left| x_i N_i \right|_{P_i} M_i \right|_M$
where $M_i = M / P_i$ and $N_i = | M_i^{-1} |_{P_i}$ is the multiplicative inverse of M_i modulo P_i.

***Mixed-Radix Conversion*:** the weighted number X can be computed by
$X = a_n \prod_{i-1}^{n}(P_i + \ldots + a_3 P_2 P_1 + a_2 P_1 + a_1)$

Where a_is are called the mixed-radix coefficients and they can be obtained from the residues by
$a_n = \left| (((x_n - a_1) \left| P_1^{-1} \right|_{P_n} - a_2) \left| P_2^{-1} \right|_{P_n} - \ldots - a_{n-1}) \left| P_{n-1}^{-1} \right|_{P_n} \right|_{P_n}$
Where $n > 1$ and $a_1 = x_1$.

For a simple 2-moduli set $\{P_1, P_2\}$, the number X can be converted from its residue representation (x_1, x_2) by
$X = a_1 + a_2 P_1 = x_1 + P_1 \left| (x_2 - x_1) \left| P_1^{-1} \right|_{P_2} \right|_{P_2}$

where $| P_1^{-1} |_{P_2}$ is the multiplicative inverse of P_1 modulo P_2.

BINARY TO RESIDUE CONVERSION

The architecture of binary to residue number system encoder based on the moduli set is represented in [8] where the binary numbers with dynamic range of proposed moduli set is $2^{3n} - 2^n$. Within this dynamic range, 3^n - bit binary number is partitioned into three n -bit parts and converted to standard residue numbers representation. this approach enables a unified design for the moduli set adders.

The available architectures for binary-to-residue encoder based on the special three moduli-set $\{2^n-1,\ 2^n,\ 2^n+1\}$ are presented here. Dynamic range corresponding to the product of the modulus for this particular moduli set is evidently $M = 2^{3n} - 2^n$ i.e. corresponds to 3n bits. Thus, given a bit unsigned binary integer , the residues corresponding to three moduli can be uniquely represented in RNS by a set of residues X =(x1, x2, x3), where x1 is the reminder when X is divided by modulo 2^n-1 denoted as $x1=(X)_{2^n}-1$, $x2=(X)_{2^n}$,. $x3=(X)_{2^n}+1$. Based on the definition of RNS, the residue is smaller than its corresponding modulo. It is well known that a bit integer in the range 0<=X<= M-1 can be represented in power-of-two notation as [8]:

$$X = \sum_{i=0}^{3n-1} b_i 2^i = N_2 \times 2^{2n} + N_1 \times 2^n + N_0$$

where

$$N_0 = \sum_{i=0}^{n-1} b_i \times 2^i, \quad N_1 = \sum_{i=n}^{2n-1} b_i \times 2^{i-n},$$

$$N_2 = \sum_{i=2n}^{3n-1} b_i \times 2^{i-2n}$$

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In order to obtain the RNS representation of the integer , partitioned into three n-bit parts N0, N1, N2 , and , three converters are required, one for each channel. The design of each channel converter are shown in Fig 1 and Fig 2 [8].

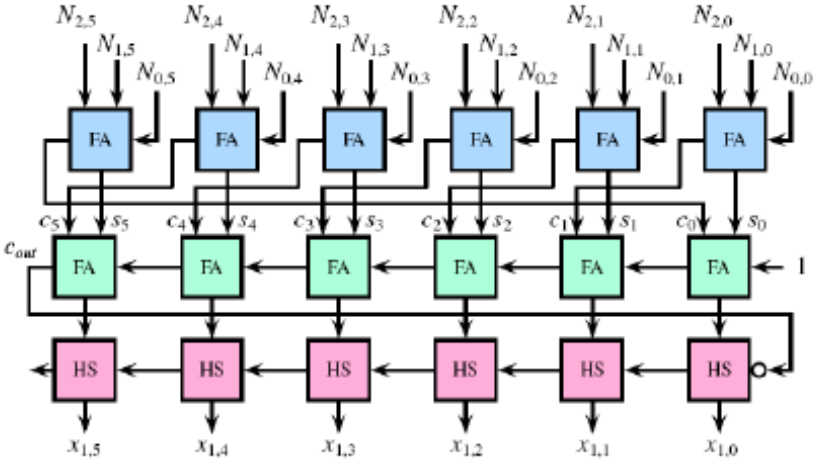

Fig.1, Binary to Modulo (2^6-1) Converter

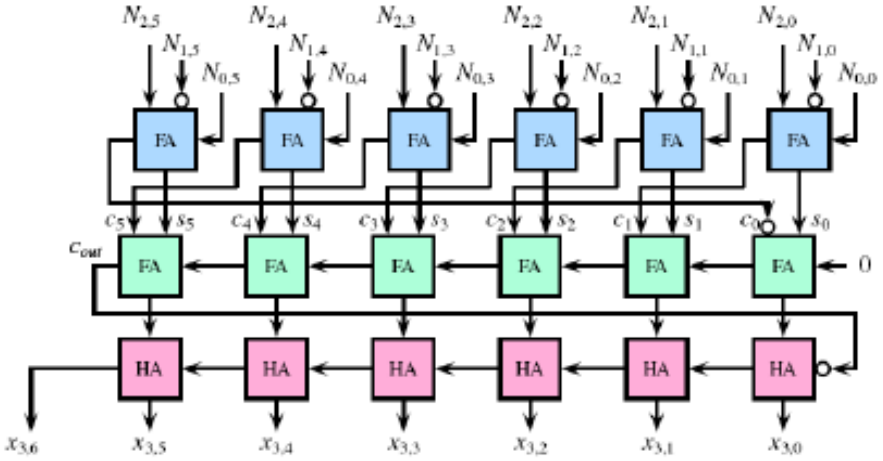

Fig.2, Binary to Modulo (2^6+1) Converter

QUINARY TO RESIDUE CONVERSION

As we have seen in last paragraph that conversion from binary to residue it needs lots of binary adders, comparators, gates and that may lead to chip complexity, propagation delay, problems of interconnections due to the big number of binary lines. One of the best solutions of the listed problems is to transfer to MVL to residue conversion. The quinary system [9] which is of the base 5 compared to base 2 of binary, will consist the most preferable approach since many researchers have been treated the quinary arithmetic and logic operations in order to compete with binary system. As known, the quinary set is {0,1,2,3,4} while binary set is {0,1}. For example, the decimal number 124 will be equal to 11100 while in quinary it is equal to 444. the representation in binary it will needs 5 digits while in quinary it will needs 3 digits only and that in fact will reduce the number of elements and number of connections hence the timing delay. In the next paragraphs, we will design the Quinary to Residue converter based on the moduli set $\{5^n - 2, 5^n - 1, 5^n\}$ and as a special case, we will study the set where n = 2 then the moduli set becomes {23, 24, 25}. The set of decimal numbers that can be converted into RNS with unique representation is {0,1,2,.....13799} which is equivalent to {0,1,2,..420144} so we need a quinary number with 6 digit inputs while RNS will be also 6 digits.

1) Three digits quinary into RNS converter:

In this case, the maximum quinary number that can converted is 124 (444).

Table I, gives the representation of decimal numbers from (0 to 124) in both quinary and RNS systems

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TABLE I. 3 DIGITS QUINARY TO RNS CONVERSION

Decimal	Quinary Number			RNS Numbers					
Number	Q2	Q1	Q0	Moduli 23		Moduli 24		Moduli 25	
	N3	N2	N1	X6	X5	X4	X3	X2	X1
0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	1	0	1	0	1
2	0	0	2	0	2	0	2	0	2
3	0	0	3	0	3	0	3	0	3
4	0	0	4	0	4	0	4	0	4
5	0	1	0	1	0	1	0	1	0
6	0	1	1	1	1	1	1	1	1
7	0	1	2	1	2	1	2	1	2
8	0	1	3	1	3	1	3	1	3
30	1	1	0	1	2	1	1	1	0
31	1	1	1	1	3	1	2	1	1
32	1	1	2	1	4	1	3	1	2
33	1	1	3	2	0	1	4	1	3
54	2	0	4	1	3	1	1	0	4
55	2	1	0	1	4	1	2	1	0
56	2	1	1	2	0	1	3	1	1
57	2	1	2	2	1	1	4	1	2
58	2	1	3	2	2	2	0	1	3
79	3	0	4	2	0	1	2	0	4
80	3	1	0	2	1	1	3	1	0
81	3	1	1	2	2	1	4	1	1
82	3	1	2	2	3	2	0	1	2
83	3	1	3	2	4	2	1	1	3
84	3	1	4	3	0	2	2	1	4
85	3	2	0	3	1	2	3	2	0
86	3	2	1	3	2	2	4	2	1
117	4	3	2	0	2	4	1	3	2
118	4	3	3	0	3	4	2	3	3
119	4	3	4	0	4	4	3	3	4
120	4	4	0	1	0	0	0	4	0
121	4	4	1	1	1	0	1	4	1
122	4	4	2	1	2	0	2	4	2
123	4	4	3	1	3	0	3	4	3
124	4	4	4	1	4	0	4	4	4

To find the logic circuit of this converter, we should refer back to the truth table or previous conversion table from Quinary to RNS. The inputs are N1, N2 and N3 while the outputs are X1, X2, X3, X4, X5 and X6.

From table I, we can deduce the following arithmetic equations:

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X1 = N1
X2 = N2
X3 = X1 + N3
(except the case when Inp1 = Inp2 = 4. In this case X3= 0)

X4 = X2 + Carry of (X1 + N3)
X5 = N3 + X3 + Carry of Comparator 1. X1, X2
X6 = X4 (comparator 2) + Carry of Comparator 2+ Carry of X5.

Based on the above equations, the logic circuit of this converter will be shown as per the figure 3

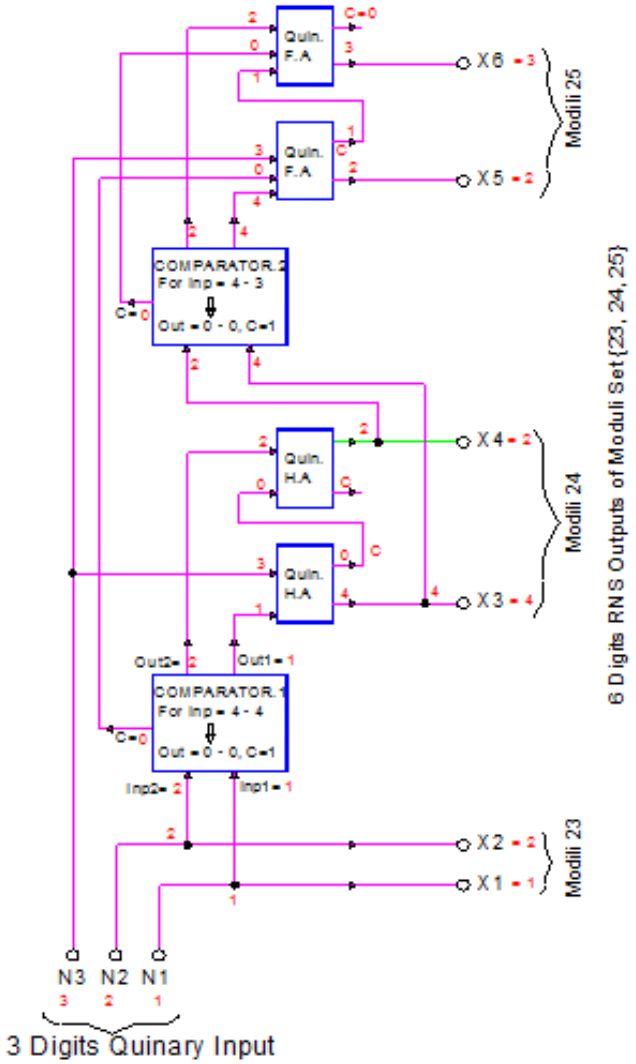

Fig.3, 3 Digits Quinary to RNS Converter

The logic circuit is consisted of six quinary components only (2 comparators, 2 half adders and 2 full adders)
To prove the conversion operation of this circuit let's take the decimal number 86 which is equivalent to 321 so N1=1, N2=2, N3=3. According to the circuit and equations:

X1 = N1 = 1
X2 = N2 = 2

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As N2N1 # to 4,4 then the outputs of comparator 1 will equal X1 = 1, X2 = 2 and the carry of comparator 1 = 0
X3 = X1 + N3 = 1 + 3 = 4
X4 = X2 + Carry of X3 adder = 2 + 0 = 2

As the inputs of Comparator-2 is (2 - 4) which is different to 4-3 then the outputs of this comparator will be 2-4 without any carry. then
X5 = N3 + X3 + Carry of comparator 1 = 3 + 4 + 0 = 2 and give Carry 1
X6 = X4 + Carry X5 + Carry Comparator 2 = 2 + 1 + 0 = 3

The final result of outputs X1,X2,X3,X4,X5,X6 is from right to left: 32 24 21which is the same result in table 1 that correspond to decimal 86 or quinary 321.

.2) Four digits quinary into RNS converter:

In this case, the maximum quinary number that can converted is 624 (4444) it means that we need 4 digits to represent each quinary input (N4 N3 N2 N1) while RNS outputs will remain with 6 digits. The Table III, gives the representation of decimal numbers from (0 to 624) in both quinary and RNS systems. From table II, we can simply notice that each quinary number (N4 N3 N2 N1) can be written as (N4 0 0 0) + (0 N3 N2 N1) then the results of residues of both numbers will be summed together to get the equivalent RNS of N4 N3 N2 N1. 0 N3 N2 N1 it is a 3 digits Quinary number and as seen in the previous section that its converter was found easily. Now let's find the converter of 4 digits quinary in the form of N4 0 0 0 where N4 = {0, 1, 2, 3, 4}. Table II, gives the representation of N4 0 0 0 quinary numbers.

TABLE II, 4TH DIGIT QUINARY TO RNS CONVERSION

Decimal	Quinary Number				RNS Number					
					Moduli 23		Moduli 24		Moduli 25	
Number	Q3	Q2	Q1	Q0						
	N4	N3	N2	N1	X6	X5	X4	X3	X2	X1
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
125	1	0	0	0	2	0	1	0	0	0
250	2	0	0	0	4	0	2	0	0	0
375	3	0	0	0	1	2	3	0	0	0
500	4	0	0	0	3	2	4	0	0	0

According to table 3, The equations of X1 to X6 will be:
X1" = X2" = X3" = 0
X4" = N4
X6" = N4 + N4
X5" = Carry of X6' + 1
So, the logic circuit of this fourth quinary digit N4 is shown in the next figure 4.

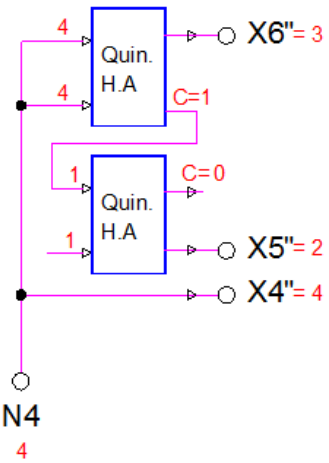

Fig. 4, 4th Digit to RNS Converter

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The combination of the fourth digit converter with the three digits converter, will give the 4 digits quinary to RNS converter. The block diagram of this converter is shown in figure...

Applying an example of a number 586 = 500 + 86
From figure 5, we found that result of conversion is 21 20 21 which is the same result of the conversion table.

TABLE III, 4 DIGITS QUINARY TO RNS CONVERSION

Decimal	**Quinary Number**				**RNS Number**					
Number	**Q3**	**Q2**	**Q1**	**Q0**	**Moduli 23**		**Moduli 24**		**Moduli 25**	
	N4	**N3**	**N2**	**N1**	**X6**	**X5**	**X4**	**X3**	**X2**	**X1**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
1	0	0	0	1	0	1	0	1	0	1
2	0	0	0	2	0	2	0	2	0	2
3	0	0	0	3	0	3	0	3	0	3
4	0	0	0	4	0	4	0	4	0	4
5	0	0	1	0	1	0	1	0	1	0
6	0	0	1	1	1	1	1	1	1	1
7	0	0	1	2	1	2	1	2	1	2
8	0	0	1	3	1	3	1	3	1	3
9	0	0	1	4	1	4	1	4	1	4
10	0	0	2	0	2	0	2	0	2	0
11	0	0	2	1	2	1	2	1	2	1
248	1	4	4	3	3	3	1	3	4	3
249	1	4	4	4	3	4	1	4	4	4
250	2	0	0	0	4	0	2	0	0	0
375	3	0	0	0	1	2	3	0	0	0
376	3	0	0	1	1	3	3	1	0	1
499	3	4	4	4	3	1	3	4	4	4
500	4	0	0	0	3	2	4	0	0	0
501	4	0	0	1	3	3	4	1	0	1
586	4	3	2	1	2	1	2	0	2	1
624	4	4	4	4	0	3	0	0	4	4

To prove the equations let's take the decimal 500 which is equivalent to 4000 (form of N4 0 0 0)
X'1 = X'2 = X'3 = 0
X4' = N4 = 4
X6' = 4 + 4 = 3 (carry = 1)
X5' = 1 + 1 = 2
then the RNS of 4000 is 3 2 4 0 0 0 (which is the in the table of conversion)

Now, if we take the decimal 586 which is (4321 = 4000 + 0321) according to the example 1 & 2 the RNS1 of 4000 = 3 2 4 0 0 0 and the RNS2 of 321 = 32 24 21

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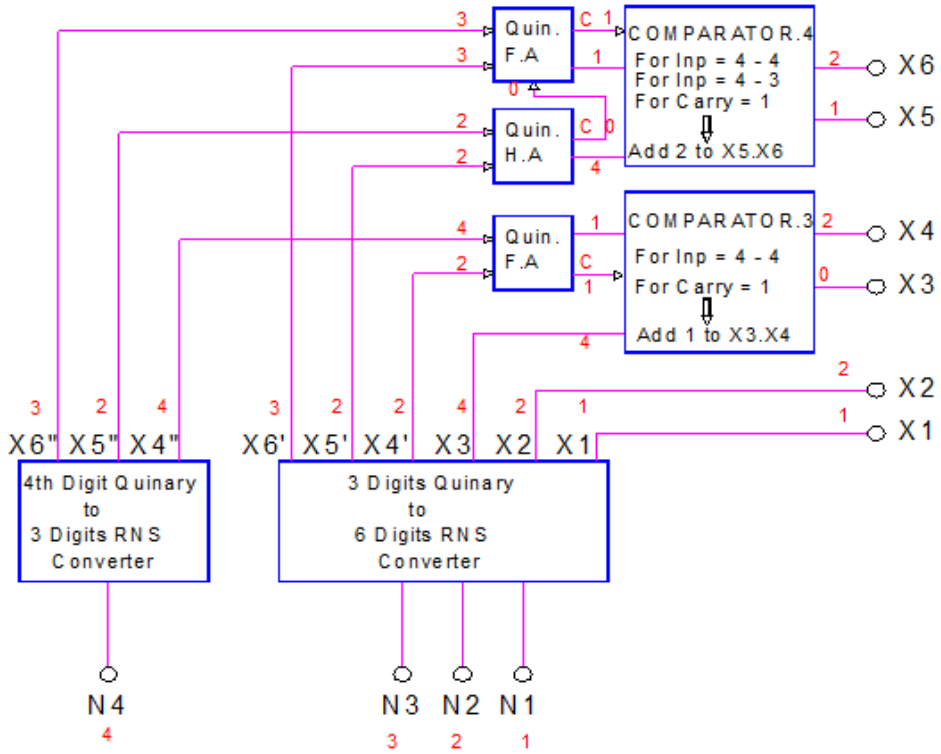

Fig. 5, 4 Digits to RNS Converter

the summation of RNS.1 and RNS.2 without carry propagation will give the RNS of 586
32 24 21
32 40 00

we will get three pairs of additions

a) (32 + 32) for moduli 23, the result is true if less than or equal quinary 42 and no carry and in case 43, 44 or getting carry then result should be subtracted by quinary 43.
   32 + 32 = 1 1 4 - 4 3 = 1 1 4 + complement 1 2 = 2 1
b) (24 + 40) = 1 1 4 - 44 = 1 1 4 + complement 1 1 = 2 0
c) (21 + 00) = 21 it is always equal to input.

So, the result is = 21 20 21 = RNS of decimal 86 (table) 4321

To convert a the number 5586 .... (44444) that includes 6 quinary digits, we can generalize the previous algorithm and the previous block diagram
where 444444 = 400000 + 40000 + 4444

RESULTS AND DISCUSSION

In this section, the amount of hardware needed for implementation of the proposed 6 digits quinary to RNS is discussed in comparison with 16 bits Binary to RNS converter [8].

a) The moduli set of binary to residue for 16 bits is {63,64,65} which is much bigger than the moduli set that used in quinary {23,24,25}. In other words, the execution of arithmetic operation in quinary will be much faster and easier than binary.
b) The number of quinary elements used in this converter is 27 (half adder, full adder, comparator) while the used elements in binary to RNS is 36. hence there is a saving in chip area around 25% and that lead also to less complexity in interconnection and also less power consumption.

CONCLUSION

In this paper, we investigate Quinary-to-residue memory less converter, which is an important issue concerning the utilization of RNS number system in DSP application. First we demonstrate a 3 digits Quinary-to-residue encoder based on the special moduli set . Next, we propose a general block diagram for a converter with higher

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capacity of quinary inputs. Comparing to Binary to Residue [8], we found that proposed algorithms and circuits lead to great reduction in elements and interconnections hence a reduction in cost and in power consumption.

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