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IMPLEMETATION OF A HIGHER ORDER SDM WITH MULTI BIT QUANTIZER

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ABSTRACT

This paper presents the fundamentals of Analog to Digital Conversion using the Sigma Delta Modulation concept. It has been clearly shown how the process of Sigma Delta Conversion used in ADCs can achieve higher speeds even after employing Oversampling above Nyquist rate. The various parameters affecting the design and performance of the Delta Sigma employed ADC have been analyzed. Stability considerations of higher order sigma delta modulators have also been analyzed to attain an optimized approach to decide upon the design of the SDM. Variation in the SNR has been shown with changes in Over Sampling Rate.

KEYWORDS: Sigma delta modulator, Over Sampling Rate, Signal to Noise Ratio, Dynamic Range, Quantization Noise

INTRODUCTION

Although real world signals are analog, it is often desirable to convert them into the digital domain using an analog to digital converter (ADC). Signal processing in the digital domain is useful in digital storage, biomedical applications, and industrial applications - from instrumentation to communication. Sigma Delta Modulators achieve a high degree of insensitivity to analog circuit imperfections, thus making them a good choice to realize embedded analog-to-digital interfaces. Application based and sophisticated design techniques demand Radio Frequency Identification Techniques which find its application in object tracking, etc. Sigma Delta ADC is high resolution ADC and acts as a major building block in RFID applications. [1] As per the sampling frequency, ADC is classified into two categories: Nyquist ADCs and Sigma- Delta ADCs. Nyquist ADCs have a lower effective number of bits due to process variation and mismatching [2]. One technique, Sigma Delta modulation, which is based on the combination of oversampling and quantization error shaping techniques, has become quite popular for achieving high resolution and high accuracy. [3] One significant advantage of the method is that analog signals are converted using only a 1-bit ADC and analog signal processing circuits having a precision that is usually much less than the resolution of the overall converter. Using sigma-delta A/D methods, high resolution can be obtained for only a low to medium signal bandwidths. The Oversampling behavior of the Sigma Delta Modulator restricts the bandwidth which can be overcome by using higher order architecture.

The Signal to Noise Ratio of Sigma Delta Modulator is dependent upon the number of bits of quantizer and is independent of amplitude of input signal. The N - bit quantizer has 2 levels and separated by V LSB. The amplitude of full scale sine wave input is 2^{N-1} V LSB. Peak to peak value is given by 2^N V LSB Mean Square Value of the Signal is given by:

$$S = (2^{N-1}V_{LSB})^2 / 2 \qquad\qquad (1)$$

Mean squared Noise is given by the expression:
$$N = V^2_{LSB}/12 \qquad\qquad (2)$$

Therefore,
Signal to Noise Ratio (SNR) is given by:
$$[(2^{N-1}V_{LSB})^2 / 2] / [V^2_{LSB}/12] \qquad\qquad (3)$$

which reduces into
$$SNR = 12^{2N} \qquad\qquad (4)$$

Also,

SNR = 6.02 N + 1.76 dB   (5)

SYSTEM DESIGN

The proposed system design is given by:

Firstly, initial parameters are defined like Over Sampling Ratio and Number of Quantization bits. In the next step, as per the order of Sigma Delta Modulator, loop filter parameters i.e. Signal Transfer Function and Noise Transfer Function are designed. Then input signal is defined for simulation of Sigma Delta Modulator through which performance parameters like Signal to Noise Ratio and Effective Number of bits are calculated. The stability of Sigma Delta Modulator depends upon loop filter parameter, and input signal amplitude. So, for designing a stable Sigma Delta Modulator, these parameters are considered.

The transfer function *Lo(z)* and Li(z) can also be realized by using feed forward signal paths to create the zeros of the NTF.

The transfer function of the feedback filter is

$$L_1(z) = -a_1 I(z) - a_2 I(z)^2 - \ldots - a_n I(z)^n \qquad (6)$$

Where $I(z)$ is the delaying integrator's transfer function

The signal filter function is

$$L_0(z) = b_1(a_1 I + \ldots \; a_n I^n) + b_2(a_2 I + \ldots \; a_n I^{n-1}) + b_{n+1} \qquad (7)$$

Considering $b_2 = b_3 = \ldots \quad b_n = 0$ and $b_1 = b_{N+1} = 1$

.

Therefore, $L_0(z) = 1 - L_1(z)$ and STF=1,

We get and provides STF = 1. Thus, the loop filter does not process the input signal u(n) , and hence this configuration has the low-distortion property.

Start

Define the values of oversampling ratio (OSR) and quantization level (QEL) for a particular level SDM-ADC

Design Loop filter through Signal Transfer Function and Noise Transfer Function according to the Order and Configuration of the Sigma Delta Modulator

Define Input Signal and Initialize parameters for the (Sigma Delta Modulator) SDM based ADC

Apply the input to the designed SDM

Vary the over sampling ratio and obtain different values of Signal to Noise Ratio (SNR)

Check the stability of the designed SDM-ADC using pole-zero plot. Is the system stable?

No

Yes

Tabulate the values of SNR by varying OSR for a same order of the SDM-ADC

Plot the analog and digital counterpart in time domain

Plot the frequency spectrum to observe the in-band residual ripple present in the output waveform
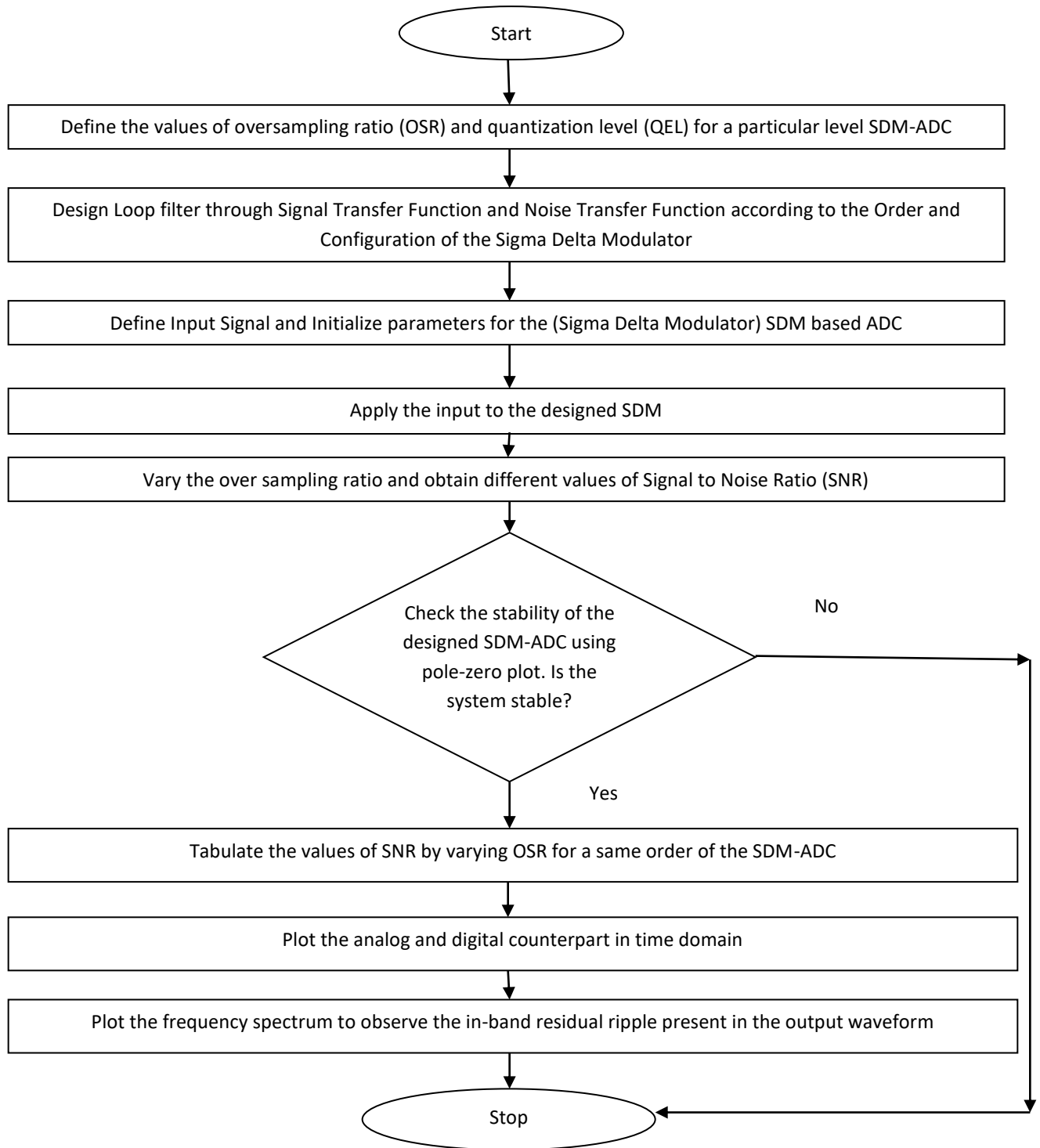
Stop

Fig.1: Flow Chart for Designing the Sigma Delta Modulator

In this work, Sigma Delta Modulator is designed by using DelSig toolbox of MATLAB. Lower order Sigma Delta Modulator i.e. First order and Second order are designed using single loop and multi bit quantizer. For designing higher order Sigma Delta Modulator from available loop filter architectures.

RESULTS

This section will deal with the comparative analysis of fourth order Sigma Delta Modulator with respect to different topologies for parameters like signal to noise ratio and effective number of bits. For realization initial parameters are taken for all topologies as OSR = 4, out of band gain (OBG) = 1.5, Quantization Level=7. A comparison of different parameters is done for different values of OSR. For the CIFB topology, Figure 5.12 gives the Realization of STF and NTF in voltage, Figure 5.13 shows the Realization of STF and NTF in dB, Figure 5.14 shows the time domain simulation of fourth order Sigma Delta Modulator , Figure 5.15 shows the integrator states of fourth order Sigma Delta Modulator where x1 is the output of first integrator, x2 is the output of second integrator, x3 is the output of third integrator, x4 is the output of fourth integrator and Figure 5.16 shows the frequency domain simulation of fourth order Sigma Delta Modulator.
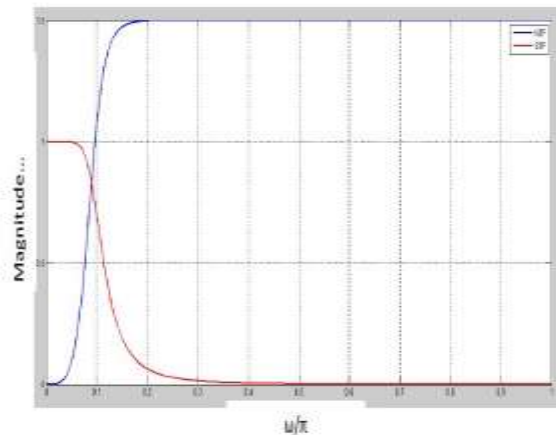

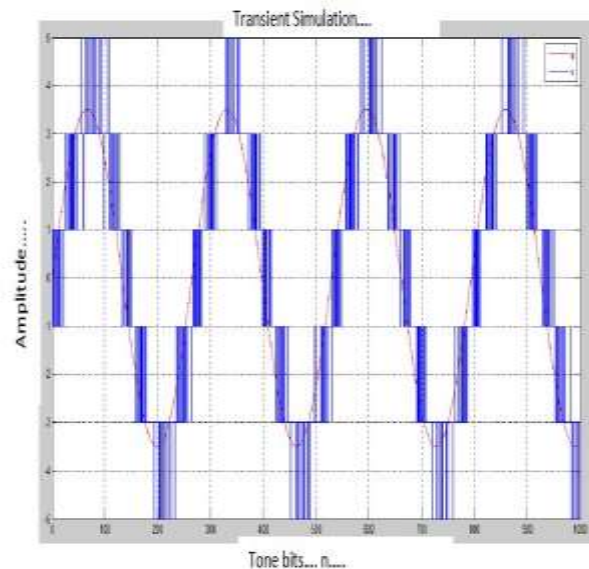**Fig.2 Realization of STF and NTF in voltage**

Fig.3 Time Domain Simulation Of Fourth Order Sigma Delta Modulator With CIBF Architecture
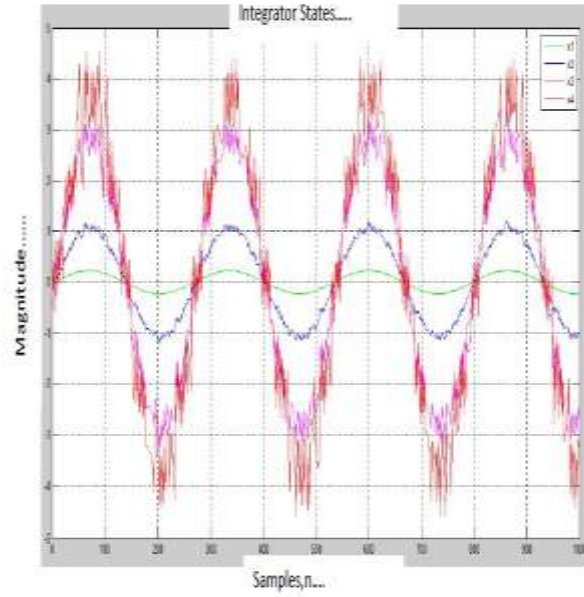
Fig.4 Integrator States Of Fourth Order Sigma Delta Modulator With CIBF Architecture
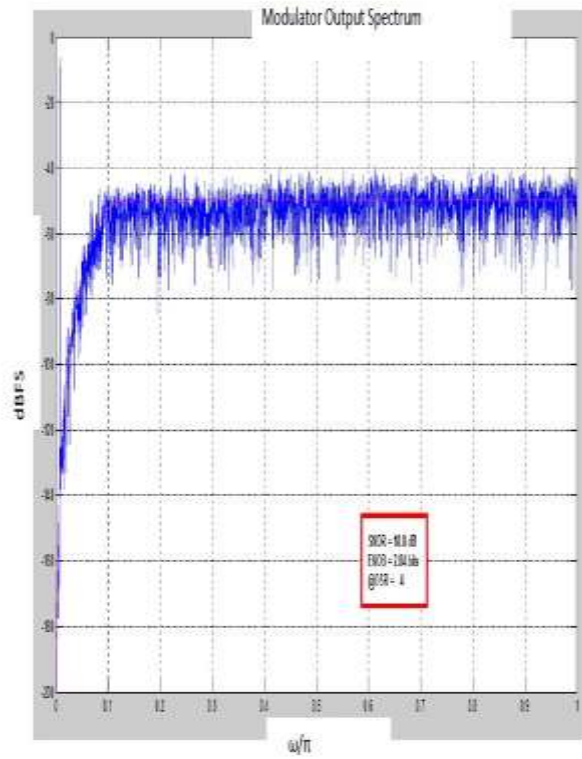

Fig.5 Frequency Domain Simulation Of Fourth Order Sigma Delta Modulator With CIBF Architecture

Sr. No.	OSR	SNR	ENoB
1	2	14.1	2.04
2	4	18.8	2.84
3	8	25.7	3.98
4	16	47.1	7.53
5	32	74.3	12.05
6	64	103.6	16.92
7	128	137.4	22.53

Table.1 Analysis Of Fourth Order Sigma Delta Modulator For Signal To Noise Ratio And Effective Number Of Bits .

Thus the aforesaid discussions along with the relevant waveforms and tables are self explanatory for the performance of higher order sigma delta modulators. The above comparative analysis concludes that parameters affecting the performance of Sigma Delta Modulator like Signal to Noise Ratio and Effective Number of Bits increases with increase in Over Sampling Ratio. Also, with the increase in order of modulator and quantization level, high SNR can be achieved at low OSR value. But with the increase of order, the modulator becomes unstable and also, maximum usable input signal amplitude decreases. The stability can be achieved for high order Sigma Delta Modulator by keeping the gain of Noise Transfer Function to be low. So, low order Sigma Delta Modulator with high OSR can be used for application.

By the use of uniform quantizer, the performance of Sigma Delta Modulator increases drastically. Stability issues can be resolved by using multibit quantizers. But the designing of multibit quantizer is complex. Also its implementation in chip is quite cumbersome, with respect to large scale integration technologies. The stability of loop filter depends upon number of factors like maximum input signal range, position of poles of Noise Transfer Function in unit circle, gain value of the loop filter etc.

So, by considering all the above parameters as per the application, the Sigma Delta Modulator of specific architecture with required order can be used. If the bandwidth requirement is modest, then conventional model of Sigma Delta Modulator of low order can be used. The Analog to Digital Converters required for audio signals which are having higher bandwidth can use Sigma Delta Modulator of higher order.

CONCLUSION

In this work, analysis of lower order and higher order Sigma Delta Modulator has been done on the basis of Signal to Noise Ratio and Effective Number of Bits. The noise shaping property of Sigma Delta Modulator has made it popular in the application where high Signal to Noise Ratio is desired. The significant property of noise shaping, pushes the noise in the range out of band of interest which reduces the requirement of sharp cut off anti aliasing filter. As, the oversampling ratio increases the Signal to Noise Ratio also increases. Higher SNR values can be achieved at lower OSR also, if higher orders of modulators are used. But as the number of integrators in the modulator increases this affects in the position of poles of the Noise Transfer Function which can make the loop filter unstable. It can be concluded from the results and conclusions that the sigma delta scheme is a highly efficient technique that can be utilized for the design of Analog to Digital Converters which yield low Quantization Noise due to the noise shaping principle employed inherently in the proposed technique.

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